CLAIMS

What is claimed is:

1. A computer system, comprising:

a processor which includes a hardware branch predictor; and

a program of software instructions executed by said processor, said software instructions including conditional branch instructions and separate static branch prediction instructions;

said static branch prediction instructions include static branch prediction bits which correspond to conditional branch instructions.

2. The computer system of claim 1, wherein said program includes one static branch prediction instruction for each group of n other instructions.

3. The computer system of claim 2, wherein n is 7.

4. The computer system of claim 2, wherein said static branch prediction bits included in a static branch prediction instruction include pairs of prediction bits, each pair providing prediction information for a separate instruction in said group of n other instructions.

5. The computer system of claim 4 wherein said prediction information includes a member selected from the group consisting of: do not use static prediction, predict taken, and predict not taken.

6. The computer system of claim 4 wherein each pair of prediction bits corresponds to another instruction and each pair of prediction bits is encoded as: 00 and 01 mean do not use static prediction, 10 means predict taken and 11 means predict not taken.

7. The computer system of claim 1 wherein said static branch prediction bits include static branch prediction information that includes encoded information directing the processor to ignore the predictions supplied by the hardware branch predictor.

8. The computer system of claim 1 wherein said hardware branch predictor includes a log in which the results of all executed conditional branch instructions are stored.

9. A processor, comprising:

fetch logic that fetches program instructions from a source external to said processor;

a dynamic branch predictor coupled to said fetch logic, said dynamic branch predictor supplies predictions regarding conditional branch instructions to said fetch logic;

an instruction queue coupled to said dynamic predictor, said fetch logic storing fetched instructions in said instruction; and

an execution unit coupled to said instruction queue and executing instructions provided from said instruction queue;

said fetch logic examines fetched instructions for a predetermined register identifier that identifies that instruction as a static branch prediction instruction that provides static branch prediction information about other fetched instructions.

10. The processor of claim 9, wherein said program instructions include one static branch prediction instruction for each group of n other instructions.

11. The processor of claim 10, wherein n is 7.

12. The computer system of claim 10, wherein said static branch prediction bits included in a static branch prediction instruction include a plurality of pairs of prediction bits, each pair providing prediction information for a separate instruction in said group of n other instructions.

13. The processor of claim 12 wherein said prediction information includes a member selected from the group consisting of: do not use static prediction, predict taken, and predict not taken.

14. The processor of claim 12 wherein each pair of prediction bits corresponds to another instruction and each pair of prediction bits is encoded by said fetch logic as: 00 and 01 mean do not use static prediction, 10 means predict taken and 11 means predict not taken.

15. The processor of claim 9 wherein said static branch prediction instruction includes branch prediction bits which encodes information directing said fetch logic to ignore the predictions supplied by the dynamic branch predictor.

16. The processor of claim 9 wherein said dynamic branch predictor includes a log in which the results of all executed conditional branch instructions are stored.

17. The processor of claim 9 wherein said predetermined identifier comprises a register identifier.

18. A method of predicting the outcome of conditional branch instructions, comprising:

(a) including a static branch predictor software instruction in a program, said branch prediction software instruction including branch prediction information pertaining to other instructions in the program;

(b) fetching said branch prediction software instructions;

(c) decoding said branch prediction software instructions to determine if said decoded instruction is a branch prediction software instruction; and

(d) if said decoded instruction is a branch prediction software instruction, then using said branch prediction information for branch prediction.

19. The method of claim 18 wherein (a) comprises including a branch prediction software instruction corresponding to a predetermined group of other instructions.

20. The method of claim 19 wherein said group includes 7 instructions.

21. The method of claim 18 wherein said branch prediction information includes pairs of bits, each pair corresponding to one of said other instructions.

22. The method of claim 21 further including decoding said pairs of bits to determine whether, for said other instruction corresponding to said pair, said other instruction is predicted taken, predicted not taken or no static branch prediction is provided.